

CONTROL CIRCUIT

Priority is claimed from U.S. provisional patent application 60/371,983 filed April 12, 2002.

FIELD OF THE INVENTION

5 The present invention relates to control circuits in television set-top boxes, and more particularly, to a feedback control circuit.

BACKGROUND

In order to achieve high-speed packet transmission, a gigabit rate transmit/receive chip set (transceiver) must be employed. One such transceiver is a
10 device sold by the Hewlett Packard Company headquartered in Palo Alto, California, USA, which makes and sells a transmitter designated as the HDMP-1022 transmitter and a receiver designated as the HDMP-1024 receiver. The HDMP-1022 transmitter and HDMP-1024 receiver chip set is described in detail in a 40-page Preliminary Technical Data sheet dated August 1996, distributed by Hewlett Packard and, at
15 present, has been available on its Internet website. This data sheet shows how the HDMP-1022 transmitter and the HDMP-1024 receiver can be utilized as a gigabit, or G-LINK™ controller, to provide transmit and receive G-LINK serial interface operations. The G-LINK of the present invention is an upgraded G-LINK II.

An application of a G-LINK controller is shown in FIG. 1, which can be used in
20 a set-top box. In the figure, a G-LINK circuit 10 serves as a serial interface circuit for coupling a conventional universal asynchronous receiver-transmitter (UART) circuit 12 to a G-LINK serial port 14 for a plurality of purposes, such as providing the UART 12 with a signal path and controls for converting from full duplex to half duplex communication to and from the G-LINK serial port 14. In addition, the G-LINK circuit

10 may relay infrared (IR) signals received from IR blaster source 20 via data line 21 for the G-LINK serial port 14 to drive an IR blaster (not shown).

All the components in FIG. 1 are controllable by an operating system (not shown) and the UART 12 is defined as a COM port. As such, when the UART 12 receives a signal, it generates an interrupt signal to be processed by the operating system. In one mode of operation such as in a configuration test mode wherein the configuration of the system is tested, the G-LINK circuit 10 forwards a test signal from the G-LINK serial port 14 to the UART 12. Under this mode of operation, the UART 12 should receive the test signal and generate interrupts accordingly.

However, in another mode of operation, such as in a demonstration mode wherein a user is educated on the use and capabilities of the system, the G-LINK circuit 10 unnecessarily transmits signals it receives from the UART 12 back to the UART 12. This unnecessary feedback causes the UART 12 to generate unnecessary interrupts to be served by the operating system. The processing of these unnecessary interrupts may degrade the performance of the set-top box. Thus, there is a need to control the communication between the G-LINK circuit and the UART 12.

SUMMARY OF THE INVENTION

According to the principles of the invention, a digital control circuit (DCC) enables/disables signals transmitted from a second circuit (such as a G-LINK circuit) to an input/output device (such as an universal asynchronous receiver/transmitter (UART)). In addition to transmitting signals to the input/output device, the second circuit also receives signals transmitted from the input/output device. The DCC may control the signals transmitted from the second circuit according to the signals transmitted by the input/output device to the second circuit. For example, when the input/output device is transmitting signals to the second circuit, the DCC inhibits

signals transmitted from the second circuit to the input/output device. This way, the input/output device does not receive any signals from the second device and thus does not generate interrupts to a central processing unit (CPU).

In one embodiment, the second circuit is a G-LINK circuit having a bi-
5 directional line coupled to a G-LINK port, and the input/output device is a UART. When the G-LINK port is short-circuited in a particular operational mode, the DCC prevents signal transmissions from the G-LINK circuit to the UART. In another operational mode, the DCC monitors the state of the UART's output and during UART transmission, the DCC sets a high state on the receive line of the UART,
10 indicating no incoming signals and thus preventing unnecessary or unwarranted UART interrupts from being generated by signals coming from the G-LINK circuit. In yet another operation mode, the DCC allows free flow of signals to be transmitted from the G-LINK circuit to the UART. The DCC thus enables the G-LINK signal feedback to the UART when required.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a prior art circuit arrangement using a G-LINK circuit, a G-LINK
20 serial port, a UART, and an IR blaster source in a set-top box;

FIG. 2 depicts a circuit arrangement according to the principles of the invention for controlling communications between the G-LINK circuit transmit line and the UART receive line;

FIGs. 3A and 3B illustrate an exemplary digital control circuit used in the circuit arrangement shown in FIG. 2 and the setup arrangements for different modes of operation;

FIG. 4 illustrates a flowchart showing the steps for entering the demonstration mode under the control of the CPU and the operating system; and

FIG. 5 illustrates a flowchart for a method for controlling transmission from a serial interface circuit to a receiver-transmitter circuit according to the mode of operation.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 2 illustrates an exemplary circuit arrangement according to the principles of the invention. A G-LINK circuit 10 serves as a serial interface circuit for coupling a conventional universal asynchronous receiver-transmitter (UART) circuit 12, e.g., a portion of a TL811 integrated circuit made by TeraLogic Inc. headquartered in Mountain View California, USA, to a G-LINK serial port 14 for a plurality of purposes, e.g., to provide the UART 12 with a signal path and controls for converting from full duplex to half duplex communication to and from G-LINK serial port 14, or to provide a signal path directly from the UART 12 to the G-LINK serial port 14 for full duplex communications, for further design improvements or for troubleshooting purposes. A digital control circuit (DCC) 22 is disposed between an output line (GLNK_Rx 18) of the G-LINK circuit 10 and a receive (input) line (UART_Rx 23) of the UART 12 for controlling the signals transmitted from the G-LINK circuit 10 to the UART 12 according to the activity present at GLNK_Tx 16 (the output line of the UART 12 or the input line of G-LINK circuit 10) and other factors discussed below.

Additionally, the present arrangement is used for the G-LINK serial port 14 to drive an infrared (IR) blaster (not shown) in response to an IR blaster source 20 via an IR blaster data line 21 coupled to G-LINK circuit 10 as shown in FIG. 2. The IR blaster is an infrared light emitting diode (LED), disposed outside of the set-top box, for controlling an external device (not shown) which can be remotely controllable by IR signals, e.g., a VCR, television receiver, DVD player, etc. The use of an IR blaster for such a purpose is known to those skilled in the art. The IR blaster source 20 is driven by a complex programmable logic device (CPLD) (not shown) and is discussed more fully below.

The circuit arrangement in FIG. 2 can also be used in a manner where paging control commands can be transmitted from the UART 12 to G-LINK serial port via the G-LINK circuit 14 for controlling an external pager module to establish a connection with a paging service provider. This circuit arrangement has been used in the ATC311 high definition televisions provided by Thomson Inc., Indianapolis, Indiana, USA.

The invention is particularly suitable for use in a set-top box (not shown) for a television receiver (not shown). Only those portions of the set-top box and/or the television receiver necessary for understanding the present invention are further discussed below. For example, the set-top box has an operating system, which in the present case is Windows CE™, a product of the Microsoft Corp. headquartered in Redmond Washington, USA, and a central processing unit (CPU) (not shown) both of which control the UART 12, the G-LINK circuit 10 and the DCC 22 discussed below. When the UART 12 receives a signal, the UART 12 generates an interrupt signal, which normally requires the operating system to jump to an interrupt handler

to process the interrupt. Other input/output or receiver-transmitter devices such a universal synchronous/asynchronous transmitter-receiver (USART) may be used in this circuit arrangement as well.

The circuit arrangement in FIG. 2 operates under several modes of operation.

5 In a configuration test mode of operation, the DCC 22 allows all the signals transmitted from the G-LINK circuit 10 to be delivered to the UART 12. In a demonstration mode, the DCC 22 disables any signals transmitted from the G-LINK circuit 10 to the UART 12. The operating system should not place the set-top box in the demonstration mode unless the operating system detects that the G-LINK serial
10 port 14 is short-circuited, which is an indication from a user that the user wants the set-top box to enter the demonstration mode. When the G-LINK serial port 14 is short-circuited, the G-LINK circuit 10 generally returns any signals that it receives from the UART 12. Thus, to detect whether the G-LINK serial port is short-circuited, the operating system may place the set-top box in the configuration test mode, send
15 a test signal to the G-LINK circuit 10 through the UART 12, and wait to see if the test signal returns from the UART 12. If the test signal returns, the operating system determines that the G-LINK serial port has been short-circuited and may proceed to place the set-top box in the demonstration mode. Short-circuiting the G-LINK serial port 14 can be achieved by shorting the plug, thereby shorting the data signal line to
20 ground.

When the G-LINK serial port 14 is not short-circuited, the set-top box normally is operating under a default mode, in which a tester by using test equipment is able to send debug messages from the UART 12 to G_LINK serial port 14. Under the default mode of operation, the G-LINK circuit 10 sends back signals it receives from
25 the UART 12, which is unnecessary. To eliminate or mask interrupts generated by

these returned signals, the DCC 22 monitors the state of the UART output line GLNK_Tx 16 and during UART 12 transmission, the UART receive line UART_Rx 23, is set to a high state, indicating to the UART 12 that no signals have been received and blocking the signals coming from the G-LINK circuit 10.

5 When the G-LINK serial port 14 is not short-circuited, the operating system may also place the set-top box in an IR blaster mode. Under this mode, the G-LINK circuit 10 generally sends signals to the UART 12. These signals are unnecessary. As such, the DCC 22 disables any signals transmitted from the G-LINK circuit 10 via GLNK_Rx 18 to the UART 12, again eliminating unnecessary interrupts.

10 The DCC hardware logic and control registers are shown in FIG. 3A. The table of FIG. 3B shows the logical behavior for the DCC 22 for each control register's setting and corresponding data inputs. In FIGs. 3A and 3B, GLNK_Rx, GLNK_Tx, and UART_Rx represent logic (signal) states at GLNK_Rx 18, GLNK_Tx 16, and UART_Rx 23, respectively. FIG. 3A shows that DCC 22 comprises five devices U1
15 through U5. U1 24 is a sequentially clocked flip-flop functioning as a latch, U2 26 and U3 28 comprise common low level logic gates, and U4 30 and U5 32 are common signal multiplexers. The DCC 22 takes the following inputs to generate UART_Rx: GLNK_Tx, GLNK_Rx, register 4 bit 3, register 6 bit 2, and register 6 bit 4. Registers 4 and 6 are included in a complex programmable logic device (CPLD) (not
20 shown) and are set by the operating system. In the following discussion, a logic value of 1 (high) generally means that no signals are transmitted. For example, when GLNK_Tx has a logic value of 1, it generally means that the GLNK_Tx 16 line is idle, i.e., not transmitting or receiving.

 U4 30 and U5 32 multiplexers provide the G-LINK circuit 10 with three
25 systems level operating modes. The simplest mode is the demonstration mode

(setup number 5 or mode 3 in FIG. 3B) where the output of U5 32 is at a logic high level – UART_Rx has a logic value of 1, i.e., the UART_Rx 23 line is idle and thus the UART 12 does not receive any signal. This mode is actuated when U5 32 has a control signal from the CPLD with register 6 bit 4 being set to a logic level 1 as shown in the table of FIG. 3B.

When register 6 bit 4 is set to a logic low level, the DCC 22 operates in one of the other two modes, or one of setup numbers 1-4. The output of U5 32 directly depends on the output of U4 30 according to FIG. 3B. U4 multiplexer is controlled by the logic level of CPLD register 6 bit 2. When the logic level of CPLD register 6 bit 2 is high, the DCC 22 operates under the configuration test mode or mode 2. In this case, the output of U4 30 is just the signals coming from GLNK_Rx 18. See FIG. 3A.

As such, the output signals at UART_Rx 23 are the same as those coming from GLNK_Rx 18. Thus, the DCC 22 enables the free flow of signals transmitted from the G-LINK circuit 10 to the UART 12. This is necessary because the test signals are generally transmitted through the G-LINK serial port 14 to the UART 12 to be processed by the operating system.

When CPLD register 6, bit 2 is set to a logic low level, the DCC 22 operates under mode 1. The output of U4 30 directly depends on the output of U3 28, which is a NAND gate having three inputs: CPLD register 14 bit 3, the signals coming from GLNK_Tx and the output signals from U2 26. U2 26 is an inverter for inverting signals coming from GLNK_Rx 18. A signal from GLNK_Tx 16 is latched at U1 24 when the signal from the GLNK_Rx 18 is transitioning from a logic value of 1 to 0. This latched state of G-LINK_Tx 16 eliminates false logic transitions at the output of U3 28 that may be due to phase or timing differences in the G-LINK_Rx 18 and G-LINK_Tx 16 signals.

Under mode 1, when CPLD register 14 bit 3 is set to a logic value of 1, the DCC 22 is in default operating condition. The DCC in this default operating condition checks whether the UART 12 is transmitting signals to the G-LINK circuit 10. If the UART 12 is not transmitting, the DCC 22 enables signals transmitted from the G-LINK circuit 10 to the UART 12. Otherwise, if the UART 12 is transmitting, the DCC 22 disables the signals transmitted from the G-LINK circuit 10. In FIGs. 3A and 3B, when the signals from GLNK_Tx 16 have a logic value of 1 (no signals), the output of U3 28 is the output of U2 26 or the signals coming from GLNK_Rx 18. In effect, the signals at UART_RX 23 are the same as those coming in at GLNK_Rx 18. On the other hand, if signals from GLNK_Tx 16 have a logic value of 0 (the UART 12 is transmitting), the output of U3 28 has a logic value of 1. In effect, the signals at UART_Rx 23 are held at a logic value of 1, disabling the transmission from the G-LINK circuit 10 to the UART 12.

Under mode 1, if CPLD register 14 bit 3 is set to a logic value of 0, the IR blaster is active, i.e., the G-LINK circuit 10 is receiving IR signals from the IR blaster source 20 and transmitting the IR signals to an external IR blaster via the G-LINK serial port 14. Under this situation, the output of U3 28 has a logic value of 1, which causes the signals at UART_Rx 23 to have a logic value of 1 as well, disabling the transmission from the G-LINK circuit 10 to the UART 12.

It should be understood that the specific level signals from the CPLD and signal levels stated in Fig. 3B are specific to the operating system used and associated circuitry, are exemplary and are presented to convey an understanding of the operation to one skilled in the art. The CPLD and its respective registers form no part of the present invention.

When a shorting plug is inserted into the G-LINK serial port 14, this short-circuiting of the output is sensed and the system is placed in the demonstration mode wherein the user is educated on the use and capabilities of the system. It is of course understood that equivalents of a shorting plug can be used, e.g., a front panel switch. This mode is typically utilized in a retail store for actuating a demonstration mode, and conforms to setup 5 of FIG. 3B. The operation of the demonstration mode forms no part of the present invention.

FIG. 4 shows a flowchart of entering the demonstration mode of operation under the control of the CPU and the operating system. When a user short-circuits the G-LINK serial port 14, the user is instructing the set-top box to enter the demonstration mode. At 402 the UART is configured as a COM port, an option provided for by the operating system. In the exemplary embodiment, the CPLD registers (not shown) are set at 404, where both bits 2 and 4 of the CPLD register 6 are set to zero, i.e., the set-top box is either in default or IR blaster mode. The process continues through link 406 to node 408 for a determination of whether the IR blaster is active. In this embodiment and as shown in FIG. 3B, if register 14 bit 3 is zero, then the IR blaster mode is active. If the IR blaster mode is active, there is a return to link 406. If "no", there is a determination at 410 of whether the operating system wants to test for whether the G-LINK serial port 14 is short-circuited (shown as "Test for DEMO PIN?") for providing a demonstration, as discussed above. If "no", there is a return to link 406. If "yes," the CPLD registers are reset at 412, setting bit 2 of CPLD register 6 to logic 1 and bit 4 to a logic 0. This setting places the circuit arrangement in FIG. 3A in the configuration test mode. At 414, the operating system determines whether the UART 12 input line, UART_Rx 23 is at a logic zero, indicating that there is signals coming into the UART 12. As discussed

above, when the serial port 14 is short-circuited, the G-LINK circuit 10 sends back any signals it receives from the UART 12. Thus, when the operating system receives a signal it previously sent, the operating system determines that the G-LINK serial port 14 is short-circuited. If the decision block 414 returns "yes", the CPLD is again
5 reset at 416 to place the circuit arrangement in FIG. 3A in the demonstration mode. As shown in FIG. 3B, to set the circuit arrangement in the demonstrative mode, bit 2 of register 2 is set to logic 0 and bit 4 is set to logic 1. The process then returns to link 406. If "no," the process returns to 404, setting the circuit arrangement back to either the default or the IR blaster alive mode.

10 FIG. 5 illustrates a method for controlling transmission from a serial interface circuit such as the G-LINK circuit 10 in FIG. 2 to a receiver-transmitter circuit such as the UART 12 in FIG. 2 in a system according to the mode of operation. At 510, the mode of the operation of the system is detected. The mode is determined at 520. If the mode is a first mode such as the configuration test mode shown in FIG. 3B, allow
15 the serial interface circuit to transmit signals to the receiver-transmitter circuit at 530. If the mode is in a second mode such as the default mode shown in FIG. 3B, determine whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit at 540. If the receiver-transmitter circuit is transmitting, prohibit the serial interface circuit to transmit signals to the receiver-transmitter at 550.

20 Otherwise, if the receiver-transmitter is not transmitting, allow the serial interface circuit to transmit signals to the receiver-transmitter circuit. As shown in FIG. 3A, the serial interface circuit may also include a bi-directional line for interfacing with a serial port (such as the G-LINK serial port 14).

The examples given herein are presented to enable those skilled in the art to more clearly understand and practice the instant invention. The examples should not be considered as limitations upon the scope of the invention, but as merely being illustrative and representative of the use of the invention. Numerous modifications and alternative embodiments of the invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the best mode of carrying out the invention and is not intended to illustrate all possible forms thereof. It is also understood that the words used are words of description, rather than limitation, and that details of the structure may be varied substantially without departing from the spirit of the invention and the exclusive use of all modifications which come within the scope of the appended claims is reserved.